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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,808	06/22/2006	Rohini Krishnan	NL03 1474 US1	6873

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EXAMINER	
WHITE, DYLAN C	
ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
08/18/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/583,808	KRISHNAN ET AL.	
	Examiner	Art Unit	
	DYLAN WHITE	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *5 and 6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 7-14* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 4/27/2009 have been fully considered but they are not persuasive.

The Examiner does not agree with all of the arguments presented based on the previous rejection. The Examiner does not concede the points made in the Office Action or agree with applicants arguments in response to the rejections made.

Regarding the applicants arguments as what a buffer can constitute, the Examiner respectfully disagrees with the applicant's remarks. The Examiner stated in the previous rejections that a series combination of two transistors (one P-type and one N-type) read on the claimed buffer circuits. The Applicant argues that the references do not disclose the transistor pairs as buffers. The references can call them what ever they wish to call them, weather it be pull up or pull down circuits, drivers, buffers, or some other terminology. A buffer circuit need only to drive a signal that was supplied to the circuit for the purpose of signal strengthening, noise reduction or other benefit of a buffer circuit. There are plenty of circuits that qualify as buffer circuits, including but not limited to inverters, non inverting buffers, comparators, and op-amps. All of these circuits while having a specific function operate within the basic definition of a buffer circuit. An inverter and a non inverting buffer circuit, in one form, are series combination of p-type and n-type transistors. The difference between the inversion and non-inversion sits in the arrangement of p-type over n-type or vice versa. For this reason

the Examiner does not agree with the applicant and stands behind the series combination of two transistors as a buffer even if the reference(s) do not specifically use the term.

Regarding the applicants arguments directed towards “determining a load" the Examiner respectfully disagrees. The applicants claim language only states a load determination means for determining a load. Any circuit that determines a load, even if it is different from what the applicant’s regard as their invention reads on the claims. The statement "determining a load" is a extremely broad term that one of ordinary skill in the art would interpret as anything that is measuring a specified load of a circuit. The Examiner does not agree with the applicants arguments directed towards the prior art references determining the load of a circuit. Furthermore the references do not have to use the exact term “determining a load” as the applicants are arguing, only that the circuit has to determine what the load is at the output pad/signal of the circuit.

With respect to the applicants arguments for switching off a buffer, this argument has been discussed before and also relates to the argument of what constitutes a buffer circuit. As the Examiner has explained the position of a series combination of at least two transistors constituting a buffer if the transistor control keeps the transistors in a non conducting state then the buffer circuit would be turned off. If there are a plurality of buffer circuits which are represented with series combination of transistors then each

individual buffer can be turned off with respect to the control signals as disclosed on the previous Office Actions.

Again the applicant argues that a pair of series connected transistors does not "typically" constitute a buffer circuit. The Examiner disagrees with this because and inverter which is a p-type transistor connected in series with an n-type transistor with a single input and an output at the node between the p-type and n-type transistors is considered a buffer. It strengthens the signal and reduces input signal noise at the circuits output. Additionally a basic non-inverting buffer circuit is where the n-type is connected in series to the p-type and outputs the same input signal on the output signal.

The Examiner also respectfully disagrees with the applicants arguments regarding switching off a buffer circuit to adjust drive capacity of a circuit. It was well known in the art that if several buffer circuits are coupled together with a common output signal, that when more buffers are turned on the drive capacity increases and when more are turned the drive capacity decreases. Adjusting the drive capacity of a circuit also relates to changing the slew rate, impedance matching the transmission line, and adjusting for fan-in/ fan-out which is based on the load just like impedance matching.

The Examiner respectfully disagrees with all of the applicants arguments with respect to the prior art. Additionally while the references may be different from the

applicants invention the applicant is claim language is broad and open to the broadest reasonable interpretation. In this case the applicant is simply claiming a means for determining load on and means for switching off a buffer circuit. There are plenty of references which read on these broad claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-8, 11 and 12-14, are rejected under 35 U.S.C. 102(b) as being anticipated by Song (U.S. Pat. 6,836,143)

Regarding claim 1, Song discloses at least one circuit component (pad 106 @ Fig. 1) at which a load is applied (resistor R) that can vary during operation (resistor R can have any value) where the configurable arrangement (107) comprises: load determination means (comparators 203 & 204) for determining a load (of resistor R) applied to the at least one configurable circuit component (105) having different fan-in or fan-out (based on the load) depending on a configuration of the circuit arrangement; adjusting means (205 and 206) for switching off a buffer (transistor pairs MP1 & MN1, MP2 & MN2, ect. @ Fig. 2A) connected to the configurable circuit (105) according to the determination (@ pad 106) of the applied load (resistor R) wherein switching off the buffer (transistor pairs MP1 & MN1, MP2 & MN2, ect.) adjusts a drive capacity (strength

of the turned on buffers) of the at least one circuit component (105) to a value less than a maximum drive value (when all buffers are not turned on) meeting a delay specification (propagation delay).

Regarding claim 2, Song discloses the determinations means (comparators 203 & 204 of 107 @ Fig. 1) is configured to determine the load (resistor R) based on configuration information (DIS based in Iref) loaded to the circuit arrangement.

Regarding claim 4, Song discloses where the configuration information (DIS) comprises a configuration bit stream (output of G10) defining at least one of an input load (resistor R) and output load of the at least one component (105).

Regarding claim 7, Song discloses where the adjusting means (205 and 206) is adapted to generate at least one control signal (UP [i:0] and DOWN [i:0]) for simultaneously (both controls signals are generated at the same time when the counters are clocked) switching off a section of buffers (transistor pairs MP1 & MN1, MP2 & MN2, ect.).

Regarding claim 8, Song discloses where the adjusting means (205 and 206) is adapted to derive the control signal (UP [i:0] and DOWN [i:0]) from a most significant bit (output of comparator) of a selection signal obtained from the determination means (203 and 204).

Regarding claim 12, Song discloses determining a load (203 & 204 @ Fig. 3) applied to at least one circuit component (pad 106) having different fan-in or fan-out (load or drive strength) depending on a configuration of the configurable circuit (107) arrangement; and switching off a buffer (transistor pairs MP1 & MN1, MP2 & MN2, ect. @ Fig. 2A) connected to the configurable circuit (107) according to the determination of the applied load (via capacitors 203 & 204), wherein switching off the buffer (transistor pairs MP1 & MN1, MP2 & MN2, ect. @ Fig. 2A) adjusts a drive capacity (strength of the turned on buffers) of the at least one circuit component (105) responsive to the determination step (capacitors 203 & 204) to a value less than a maximum drive capacity (when all buffers are not turned on) while still meeting a delay requirement (propagation delay).

Regarding claim 13, Song discloses further comprising simultaneously switching off a section of buffers (both controls signals are generated at the same time when the counters are clocked).

Regarding claim 14, Song discloses deriving the control signal (UP [i:0] and DOWN [i:0]) from a most significant bit of a selection signal (output of comparator).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schultz et al. (U.S. Pat. 6,445,245) in view of Ajit (U.S. Pub. 2002/0113628).

Regarding claim 9, Song discloses that of claim 1 but fails to teach where the adjusting means is configured to vary the threshold voltage of a circuit elements in the arrangement.

Ajit teaches (Fig. 6) changing the transistor threshold voltage by biasing the transistor wells with biasing circuit (401), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the output buffer disclosed by Song with the transistor biasing as taught by Ajit for varying the on/off voltage thresholds of the drive transistors.

Regarding claim 10, the combination discloses where the adjusting means (Ajit; 401 @ Fig. 10) is adapted to change at least one bias voltage (PMOS transistors) in response to the determination means (transistors 1001).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Song (U.S. Pat. 6,836,143) in view of Schultz et al. (U.S. Pat. 6,445,245).

Regarding claim 11, Song fails to disclose where the circuit is part of an FPGA.

Schultz discloses a configurable circuit which used load determination using comparators 303 & 403 to adjust the impedance control circuit which is used to switch off buffer circuits (transistor pairs) where the circuit arrangement is part of an FPGA (col. 1, lines 13-16), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the configurable circuit arrangement as taught by Song with the FPGA as taught by Schultz for programmable configuration after design or manufacture.

Allowable Subject Matter

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 3, Song discloses where the configuration information is stored in a configuration memory.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to output buffer circuitry and load determination.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dylan White/
Examiner, Art Unit 2819

/Rexford N BARNIE/

Supervisory Patent Examiner, Art Unit 2819